JEDEC STANDARD

Scalable Low-Voltage Signaling for 400 mV (SLVS-400)

JESD8-13

OCTOBER 2001

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by

© JEDEC Solid State Technology Association 2001
2500 Wilson Boulevard
Arlington, VA 22201-3834

Price: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)

Printed in the U.S.A.

Introduction

SLVS is a chip-to-chip signaling protocol which is designed from the beginning for maximum performance and minimum power consumption. It derives from four fundamental principles:

a) Maximum performance requires that both near- and far-end reflection coefficients be minimized. Therefore both driver and terminator impedances must closely match the line impedance.

b) For reasonable power consumption, signal swing should be as small as is consistent with receiver performance.

c) Power supply voltages will continue to decrease, as will the swing needed for receiver performance. Therefore, the signaling protocol should be as independent of the positive supply as possible.

d) Additional low-impedance supplies, especially ones that can both sink and source current, are expensive both in cost and performance impact.

Item (a) demands shunt termination. (c) and (d) rule out the positive signal supply and any third supply, which leaves ground as the termination potential. Combined with (a) this demands a signal swing between ground and 50% of the output supply, which is consistent with (c). As an added benefit, this simplifies CMOS differential receivers because they don't need to combine N- and P-channel differential inputs. (b) suggests I/O operation below the core-logic supply potential, which minimizes intergenerational incompatibility.

Higher-level data organization is outside of the scope of this specification, but it should be noted that variations in supply and ground current are incompatibile with maximum performance. For that reason, SLVS-400 is intended for use with DC-balanced data groupings such as 4B/6B and differential (1B/2B) codes.

Specific applications are also outside of this specification's scope. That said, it should be noted that ground termination greatly simplifies hot-insertion systems. It should also be noted that with a timing budget relaxed to account for line settling and L di/dt drops the source-impedance matching of SLVS-400 allows its use in unterminated (reflected-wave) switching environments.

SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400)

(From JEDEC Board ballot JCB-01-83, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified.

2 Description

SLVS-400 is a differential voltage-based signaling protocol. The nominal VOL of 0 (ground) and a nominal VOH of 400 mV. Because the driver impedance must be matched to the line and termination impedances, this requires a nominal 800 mV power supply (VDDQ). SLVS defines three primitive types: drivers, receivers, and terminators. A practical SLVS system must have at least one of each type, although it is possible and in fact quite practical for all three to be incorporated into a single node.

2.1 Drivers

An SLVS-400 driver is defined to be in one of three states:

High Impedance	Self-explanatory. Between $V_{O(MIN)}$ and $V_{O(MAX)}$ the absolute magnitude of the device current is less than or equal to $I_{L(max)}$
Low	Output Thevenin potential is V_{SSQ}; ouptut Thevenin impedance is linear and within 10% of Z_0 around the operating point of 0 V.
High	Output Thevenin potential is V_{DDQ}; output Thevenin impedance is linear and within 20% of Z_0 around the operating point of $V_{DDQ}/2$.

2 Description (cont'd)

2.2 Receivers

An SLVS-400 receiver is defined to be in one of five states:

Switching High	$D_{IN}+ - D_{IN}- \geq V_{IH(AC)}$ causes the receiver to switch TRUE with specified AC timings.
Holding High	$D_{IN}+ - D_{IN}- \geq V_{IH(DC)}$ guarantees that a TRUE receiver will not switch FALSE.
Undefined	All bets are off.
Holding Low	$D_{IN}+ - D_{IN}- \leq V_{IL(DC)}$ guarantees that a FALSE receiver will not switch TRUE.
Switching Low	$D_{IN}+ - D_{IN}- \leq V_{IL(AC)}$ causes the receiver to switch FALSE with specified AC timings.

2.3 Terminators

SLVS-400 terminators are identical to SLVS-400 drivers in the LOW state, which is quite convenient for bidirectional links and for preventing high-frequency stubs in receivers.

3 Parametrics

SLVS-400 currents and impedances are specified in the context of odd-mode transmission-line impedances between 50 and 62 ohms (56 Ω ± 10%). In the interest of standardization implementors should attempt to conform to this range, but the whole point of SLVS is scalability and this applies to impedances as well as supply potentials. For lower or higher line impedances, the currents specified herein should be scaled linearly.

3.1 Power Supply

SLVS-400 uses only one power supply:

	Minimum	Maximum	Units
V_{DDQ}	750	850	mV

3 Parametrics (cont'd)

3.2 Terminator parametrics

Terminators have two critical operating points:

- the static HIGH operating point, where the terminator sets the steady-state current flowing in the line; this is the I_{TH} operating point.

- the dynamic LOW operating region, where the terminator impedance ($R_{DS(ON)}$) determines the line damping factor; this region is bounded by the I_{TL1} and I_{TL2} operating points.

	Minimum @ Voltage		Maximum @ Voltage	
I_{TH}	8.0 mA	500 mV	6.4 mA	320 mV
I_{TL1}	3.0 mA	200 mV	4.5 mA	200 mV
I_{TL2}	-3.0 mA	-200 mV	-4.5 mA	-200 mV
Z_{TH}	44 Ω (Note 1)		68 Ω (Note 1)	
Z_{TL}	44 Ω (Note 2)		68 Ω (Note 2)	

NOTE 1 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between 320 mV and 500 mV

NOTE 2 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between -200 mV and 200 mV

3.3 Receiver parametrics

Although performance requirements dictate that SLVS systems maintain balanced currents in both the driver and terminator devices, this does not necessarily mean strict differential (1B/2B) signaling. It is possible to save pins while maintaining DC balance using 4B/6B and 6B/8B coding as well, while using the mean potential of the code group as a receiver reference. The drawback to the non-differential coding schemes is that they have less than half of the signal amplitude at the receiver compared to differential signaling. SLVS receiver class I is sensitive enough to operate in this environment, while SLVS receiver class II requires the full differential input signal swing.

3.3 Receiver parametrics (cont'd)

3.3.1 Class I receivers

Class I receivers compare a single-ended input to a shared reference, V_{REF}.

	Minimum	Maximum	Notes
V_{REF}	120 mV	280 mV	1
$V_{IL(AC)}$	-300 mV	V_{REF}-90 mV	
$V_{IL(DC)}$	-300 mV	V_{REF}-50 mV	
$V_{IH(DC)}$	V_{REF}+50 mV	1150 mV	
$V_{IH(AC)}$	V_{REF}+90 mV	1150 mV	
V_{IX}	100 mV	300 mV	2

NOTE 1 V_{REF} generation is the responsibility of the system implementor. Deviations from the input signal crosspoint voltage (V_{IX}) will result in performance degradation.

NOTE 2 V_{IX} defines the range of input crossing points for which timing characterization remains valid.

3.3.2 Class II receivers

Class II receivers compare two differential inputs, D_{IN}+ and D_{IN}-.

	Minimum	Maximum	Notes
$V_{IL(AC)}$	D_{IN}+, D_{IN}- ≥ -300 mV	D_{IN}+ ≤ D_{IN}- - 160 mV	
$V_{IL(DC)}$	D_{IN}+, D_{IN}- ≥ -300 mV	D_{IN}+ ≤ D_{IN}- - 100 mV	
$V_{IH(DC)}$	D_{IN}+ ≥ D_{IN}- + 100 mV	D_{IN}+, D_{IN}- ≤ 1150 mV	
$V_{IH(AC)}$	D_{IN}+ ≥ D_{IN}- + 160 mV	D_{IN}+, D_{IN}- ≤ 1150 mV	
V_{IX}	100 mV	300 mV	1

NOTE 1 V_{IX} defines the range of input crossing points for which timing characterization remains valid.

3.4 Driver parametrics

SLVS-400 defines two classes of drivers. Class A drivers are intended for point-to-point operation, so the load seen by the driver is nominally Z_0. Class B drivers are intended for multidrop bus operation; the load seen by them is $Z_0/2$. Since the endpoint devices in a multidrop environment effectively drive a single line (notably when they double as terminators when not driving the line) they can be Class A. In practice many implementations will allow for class selection.

3.4.1 Class A drivers

	Minimum	Maximum	Notes
V_{OH}	320 mV @ -6.4 mA	500 mV @ -8.0 mA	
I_{OLP}	3.0 mA @ 200 mV	4.5 mA @ 200 mV	
I_{OLN}	-3.0 mA @ -200 mV	-4.5 mA @ -200 mV	
Z_{OH}	44 Ω	68 Ω	1
Z_{OL}	44 Ω	68 Ω	2
V_{OX}	0.4 V_{OH}	0.6 V_{OH}	3

NOTE 1 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between 320 mV and 500 mV

NOTE 2 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between -200 mV and 200 mV

NOTE 3 Output crosspoint voltage must remain within the specified limits relative to V_{OH} for balanced loads of between 50 and 62 ohms to ground.

3.4 Driver parametrics (cont'd)

3.4.2 Class B drivers

	Minimum	Maximum	Notes
V_{OH}	320 mV @ -12.8 mA	500 mV @ -16.0 mA	
I_{OLP}	6.0 mA @ 200 mV	9.0 mA @ 200 mV	
I_{OLN}	-6.0 mA @ -200 mV	-9.0 mA @ -200 mV	
Z_{OH}	22 Ω	34 Ω	1
Z_{OL}	22 Ω	34 Ω	2
V_{OX}	0.4 V_{OH}	0.6 V_{OH}	3

NOTE 1 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between 320 mV and 500 mV

NOTE 2 Dynamic impedance (dV/di) must not exceed the specified limits for all operating points between -200 mV and 200 mV

NOTE 3 Output crosspoint voltage must remain within the specified limits relative to V_{OH} for balanced loads of between 25 and 31 ohms to ground.


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